



*15th IEEE
EUROPEAN TEST SYMPOSIUM*
Prague, Czech Republic
May 24-28, 2010



Test Spring School at ETS'10

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1. School Presentation

The European Test Symposium offers a 3 day test spring school (TSS[®]ETS) for Ph. D. and M. Sc. students which will introduce into modern test technology. Renowned experts will give lectures and will cover the main challenges of test and reliability of today's nanoelectronic systems.

Test and embedded test, manufacturability and robustness have to be considered by any system designer in order to come up with successful products. TSS[®]ETS offers the unique opportunity to learn about the leading edge of the state of the art in testing in a comprehensive and compact way. The school will give the opportunity to earn credits and a certificate by passing an exam online.

The school is organized in conjunction with ETS, and the last two lectures are open for the general ETS attendees without additional fee. TSS[®]ETS is offered to registered students at the low cost rate of appr. 200 EUR incl. food plus the 3 day accommodation for appr. 100 EUR. The school is also available for professionals at higher rates, however priority is given to students on a first come – first serve basis as the number of attendees is strictly limited.



Hans-Joachim
Wunderlich

Chair of the Steering
Committee of ETS



Paolo
Prinetto

Organization
Committee

2. Venue

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3. Registration

Registrations should be done at:

<https://amca.cz/coms-1.0/index.php/registration/tss-2010-eng>

4. Schedule

Friday, May 21	
16:00-18:00	Registration
Saturday, May 22	
7:30-8:00	Registration
8:00-8:15	Welcome Address (Hans-Joachim WUNDERLICH)
8:15-12:45	Basics on VLSI Technology in Test (Adit SINGH) Breaks: 9:30-9:45, 10:45-11:00
12:45-14:00	Lunch
14:00-18:30	Fault Models, Fault Simulation and Test Generation (Vishwani AGRAWAL) Breaks: 15:30-15:45, 16:45-17:00
18:30-	Social, Dinner
Sunday, May 23	
8:00-12:30	Defect Based Testing and Diagnosis (Michel RENOVELL) Breaks: 9:30-9:45, 10:45-11:00
12:30-14:00	Lunch
14:00-18:30	Design for Test, BIST and BISR (Jerzy TYSZER) Breaks: 15:30-15:45, 16:45-17:00
18:30-	Social, Dinner
Monday, May 24	
8:00-12:30	Reliability and Design for Manufacturing (Abhijit CHATTERJEE) Breaks: 9:30-9:45, 10:45-11:00
12:30-14:00	Lunch, Checkout, Transfer to ETS location
Track A	Infrastructure IP for SOC (Yervant ZORIAN)
14:00-18:30	Breaks: 15:30-15:45, 16:45-17:00
Track B	Test of TSV-based 3D Stacked ICs (Erik Jan MARINISSEN)
14:00-18:30	Coffeebreaks: 15:30-15:45, 16:45-17:00

Lunch: Self-service restaurant in the center

5. Basics on VLSI Technology in Test

5.1. Abstract

The testing of complex integrated circuits is extremely challenging because of the exponential nature of the problem; applying all possible input combinations to fully check a large circuit can require test time of the order of centuries, even at the fastest possible clock rates. In practice, only tiny fraction of the input space can be tested in reasonable time and cost. But such a limited test must still ensure that virtually all defects in the circuit are detected so as to avoid failure during operation. This requires careful selection of the test inputs to ensure that they target all the likely circuit faults. Fortunately not all possible functional failures in a circuit are equally likely, and many are virtually impossible, making it practical to achieve high test quality without applying all possible inputs.

Targeting likely circuit faults requires an understanding of the underlying circuit structures and manufacturing technologies, and the possible sources of manufacturing and field failures. This introductory session will review the basics of CMOS technology, before moving on to discuss the types and sources of common manufacturing defects and their impact on circuit performance. Tests to detect specific types of circuit faults will be introduced. Following discussion of the traditional stuck-at, bridging, IDDQ, and transition delay test approaches, challenges posed by state-of-the-art nanometer technologies such as latent faults, small delay defects, and random performance variability will also be presented.

5.2. Schedule

Saturday, May 22 : 8:15-12:45

5.3. Speaker

Adit SINGH

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5.3.1. Biography

Adit D. Singh received the B.Tech from IIT Kanpur, and the M.S. and Ph.D. from Virginia Tech, all in Electrical Engineering.

Currently he is James B. Davis Professor of Electrical and Computer Engineering at Auburn University. Earlier, he has held faculty positions at the University of Massachusetts, Amherst and Virginia Tech in Blacksburg.

His research interests span high performance VLSI systems, IC and SOC testing, and microelectronic system reliability and fault tolerance.

He has published extensively in these areas, and holds several international patents that have been licensed to industry.

He is particularly recognized for his pioneering contributions to statistical methods in test and adaptive testing. In addition to extensive support from US the National Science Foundation, his research has also been supported by the Max Plank Society of Germany, and the Fulbright Foundation.

He is a very popular lecturer and over the years has been invited to present over sixty technical courses at international conferences, and in-house in companies.

Dr. Singh currently serves as Chair of the IEEE Test Technology Technical Council, and on the editorial boards of IEEE Design and Test Magazine and the Journal of Test and Test Applications (JETTA).

He has held leadership positions in dozens of technical conferences, most recently serving as Co-General Chair for the 2010 IEEE International Workshop on Reliability Aware Design and Test (RASDAT-10), and Co-Program Chair of the 2009 IEEE international Workshop on Design for Variability and Reliability (DRV09).

He is a Fellow of the IEEE, and a “Golden Core” member of the IEEE Computer Society.

5.4. Syllabus

1. Introduction
2. The evolution of IC technologies
3. CMOS circuit structures
4. Overview of CMOS processing
5. Technology scaling and advanced materials
6. Manufacturing defects and the yield challenge
7. The importance of testing to ensure product quality

8. The exponential complexity of test
9. Reducing test set size by targeting logical faults
10. The stuck-at-fault model
11. How good is the stuck-at fault assumption?
12. CMOS physical defects modeled with stuck open and bridging faults
13. IDDQ testing
14. Delay and timing defects and fault models
15. Process variability
16. Latent defects and the need for stress testing
17. Summary
18. Conclusion and discussion.

6. Fault Models, Fault Simulation and Test Generation

6.1. Abstract

These lectures are selected from a full-semester graduate-level university course on VLSI testing.

The student is presumed to have only basic understanding of logic circuits and introductory ideas of VLSI technology.

This set of five lectures includes simple classroom exercises and discussion on theoretical and practical aspects of VLSI testing.

The objective is to fulfill the needs of today's industrial VLSI design and manufacturing environment, which demands knowledge of testing concepts.

The presentation material is based on the textbook, M. L. Bushnell and V. D. Agrawal, *Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits*, Springer, 2000.

6.2. Schedule

Saturday, May 22 : 14:00-18:30

6.3. Speaker

Vishwani D. AGRAWAL

James J. Danaher Professor, ECE Dept.

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6.3.1. Biography

Vishwani D. Agrawal is the James J. Danaher Professor of Electrical and Computer Engineering at Auburn University, Alabama.

He has over thirty years of industry and university experience, working at Bell Labs, Murray Hill, NJ; Rutgers University, New Brunswick, NJ; TRW, Redondo Beach, CA; IIT, Delhi, India; EG&G,

Albuquerque, NM; and ATI, Champaign, IL.

His expertise includes VLSI testing, low-power design, and microwave antennas.

He obtained his BE degree from the University of Roorkee (renamed Indian Institute of Technology), Roorkee, India, in 1964; ME degree from the Indian Institute of Science, Bangalore, India, in 1966; and PhD degree in electrical engineering from the University of Illinois, Urbana-Champaign, in 1971.

He has published over 300 papers and coauthored five books.

He holds thirteen United States patents.

His textbook, Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits, co-authored with M. L. Bushnell, was published in 2000.

He is the founder and Editor-in-Chief (1990-) of the Journal of Electronic Testing: Theory and Applications, and a past Editor-in-Chief (1985-87) of the IEEE Design & Test of Computers magazine. During 2003-08, he served on the Editorial Board of the IEEE Transactions on VLSI Systems.

He is the Founder and Consulting Editor of the Frontiers in Electronic Testing Book Series of Springer.

He has received eight Best Paper Awards and two Honorable Mention Paper Awards. In 2006, he received the Life-Time Achievement Award of the VLSI Society of India, in recognition of his contributions to the area of VLSI Test and for founding and steering the International Conference on VLSI Design in India. In 1998, he received the Harry H. Goode Memorial Award of the IEEE Computer Society, for innovative contributions to the field of electronic testing, and in 1993, received the Distinguished Alumnus Award of the University of Illinois at Urbana-Champaign, in recognition of his outstanding contributions in design and test of VLSI systems.

Agrawal is Fellow of the IETE-India, Fellow of the IEEE and Fellow of the ACM.

He has served on the advisory boards of the ECE Departments at University of Illinois, New Jersey Institute of Technology, and the City College of the City University of New York.

See his website -- <http://www.eng.auburn.edu/~vagrawal>.

6.4. Syllabus

1. Fault Modeling (stuck-at and other faults)
2. Logic Simulation (modeling levels, event-driven simulation)
3. Fault Simulation (parallel, deductive and concurrent methods)
4. Combinational Circuit Test Generation (D-algorithm, Podem)
5. Sequential Circuit Test Generation (time-frame, simulation-based)

7. Defect Based Testing and Diagnosis

7.1. Abstract

Opens and Shorts defects are responsible for a large percentage of failures in CMOS technologies and their impact in nanometer technologies with highly dense interconnect structures is expected to increase. In this presentation a survey of the key developments in modelling open and short defects as well as floating gate and gate oxide short and their implications in test and diagnosis are presented. An overview of the historical developments of these models to more realistic proposals taking into consideration the unpredictable parameters of the defect such as resistance, location, etc are presented. The logic detectability of defects taking into consideration their unpredictable parameters assuring their detectability is explored. The concept of Analogue Detectability Interval (ADI) as well as its applicability to increase the quality of the vectors detecting these defect classes is introduced. Quality of electronic circuits and systems requires the availability of effective diagnosis techniques. The basic concepts of logic as well as current-based (I_{DDQ}) diagnostic strategies are included in this presentation.

7.2. Schedule

Sunday, May 23 : 8:00-12:30

7.3. Speaker

Michel RENOVELL

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7.3.1. Biography

In 1986, Michel Renovell joined the Laboratory of Computer Science, Automation and Microelectronics of Montpellier where he is a researcher funded by the French National Council for Scientific Research (CNRS).

From 1995 to 2005, he served as head of the Microelectronics team at LIRMM.

From 2006 to 2009, he served as Scientific Advisor for the National CNRS headquarter managing more than 250 labs in France. He is also Director of the "French National Network on SOC/SiP".

He is a member of the editorial board of JETTA, the editorial board of IEEE Design & Test and the editorial board of the VLSI Journal.

Michel was general chair and program chair of many conferences (ETS, VTS, DELTA, IMSTW, FPL, SBCCI, DDECS.), he has published over 150 international papers and has received several best paper awards.

His research interests include: Fault modeling, Analog testing and FPGA testing.

7.4. Syllabus

1. Test with Classical Fault Models
 - Stuck-at
 - Wired-Or
 - Wired-AND
 - Dominant
 - Stuck-Open
2. Diagnosis with Classical Fault models
 - Stuck-at
 - Wired
3. Realistic Fault Models
 - Voting
 - Biased Voting
 - Direct Voting
4. Analysis of Realistic Defect
 - Resistive short
 - Resistive Open
 - Floating gate
 - Gate Oxide Short
5. Diagnosis with Realistic Defect
6. Test with Realistic Defect Models
 - Detection Interval
 - Global Detection Interval
 - Efficiency metrics

8. Design for Test, BIST and BISR

8.1. Abstract

The rapid scaling of semiconductor devices along with technological innovations allow designers to embed more than 100 million transistors running in the GHz range. Testing designs of this complexity is a significant challenge.

This lecture will focus on some of the advances shaping the test industry to address design and process changes. In particular, we will present state-of-the-art design-for-test (DFT) methodologies and practices for high-quality low-cost manufacturing test.

In addition to scan-based testing and issues related to at-speed testing in scan environment, the lecture will cover guidelines for design of built-in self-testable cores, techniques for random pattern testability, as well as BIST architectures for random logic and memory arrays, including built-in self-repair (BISR) schemes.

The lecture will also highlight, from a DFT perspective, methods deployed both to control test power dissipation and to reduce a negative impact of unknown states on test quality.

Finally, we will illustrate applications and discuss future trends of DFT technology.

8.2. Schedule

Sunday, May 23 : 14:00-18:30

8.3. Speaker

Jerzy TYSZER

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8.3.1. Biography

Jerzy Tyszer is the Professor of Electronics and Computer Science at the Faculty of Electronics and Telecommunications of Poznań University of Technology, Poland.

His main research interests include design for testability, built-in self-test, and embedded test. He is co-inventor of the award-winning Embedded Deterministic Test (EDT™) technology used in the first commercial test compression product TestKompress®. His paper on EDT at the IEEE International Test Conference in 2002 was recognized as one of the most significant papers published in the last 35 years. He was co-recipient of the 1995 and 1998 Best Paper Awards at the IEEE VLSI Test Symposium, the 2003 Honorable Mention Award at the IEEE International Test Conference, the 2009 Best Paper Award at the VLSI Design Conference, and a very prestigious 2006 IEEE Circuits and Systems Society Donald O. Pederson Outstanding Paper Award recognizing the paper on EDT published in the *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*.

He has published 7 books, more than 100 research papers and is co-inventor of 42 US and international patents.

Prof. Tyszer is co-author of *Arithmetic Built-In Self-Test for Embedded Systems*, Prentice Hall, 1997, and the author of *Object-Oriented Computer Simulation of Discrete Event Systems*, Kluwer Academic Publishers, 1999.

He is serving on technical program committees of various IEEE conferences including International Test Conference, VLSI Test Symposium, and European Test Symposium.

He received the Ph.D. degree in electrical engineering from Poznań University of Technology, Poland, in 1987.

He was with McGill University, Montreal, Canada, from 1990 to 1996 as a Research Associate and Adjunct Professor.

8.4. Syllabus

1. Introduction
Testing of sequential circuits, functional and random tests, sequential ATPG, test time
2. Why DFT?
Logic-to-pin ratio, circuit complexity, test generation time, volume of test data, performance testing, state variables, controllability and observability, ability to set internal nodes and to propagate their values to outputs, measures of circuit testability, ad hoc DFT techniques
3. Scan-based designs
Scan cells, multiplexing of data flip-flops, impact on performance, modes of operation, generic scan path, parallel scan chains, test application time, safe scan shifting, testing procedure, flush test, scan shift and capture operations, partial scan
4. Test points
Observation and control points, selection of test points, test points driven by scan, multiphase test point insertion
5. Benefits and cost of scan
Impact on controllability, observability, testability, ATPG, and fault simulation, hardware debugging and verification, fault diagnosis, area overhead, performance degradation, scan test cost
6. Low power scan-based test
Reducing power dissipation, solutions for scan testing in shift and capture, test scheduling and reordering, scan partitioning, transition blocking, clock gating, low-transition test pattern

- generators, minimum transition fill, patterns with low switching activity, low power scan operations
7. Level sensitive scan design (LSSD)
Hazard-free latches, design rules, double-latch design, single-latch design
 8. Boundary scan
Objectives, boundary scan architecture, standard IEEE 1194.1, TAP state diagram, board testing, testing of interconnects, invoking BIST functionality
 9. At-speed scan-based test
Single clock domain - single capture, over-testing, timing in capture window, frequency to reduce power and constraints on BIST controller, frequency to reduce test time, double capture, launch from a semi-legal state, slow scan enable, multiple clock domains, at-speed testing within and between clock domains, clock suppression, hold states, multiple frequencies - single capture
 10. Built-in self-test (BIST)
External testers, tester accuracy, capacity and bandwidth, test application time, cost, volume of test data, yield loss due to ATE inaccuracy, BIST principles, on chip test generation and response evaluation, devices to produce test patterns and compact test responses, BIST-ready designs, BIST-ready designs with scan, STUMPS architecture, pseudo-random testing, fault coverage by random patterns
 11. On-chip test pattern generators
Generation of pseudorandom test patterns, test sequence aperiodicity, structural and linear dependencies, driving large number of scan chains, operational speeds, linear feedback shift registers (LFSRs), primitive characteristic polynomials, m -sequence, principle of superposition, hybrid LFSR and cellular automata, ring generators, two-dimensional generators, phase shifter synthesis, weighted pseudo-random patterns, low transition PRPG
 12. Test data volume compression
Stimuli replication, stimuli encoding, static reseeding of LFSRs, solving of linear equations, compression ratios and encoding efficiency, multiple polynomial reseeding, continuous flow decompression (dynamic reseeding), embedded deterministic test, low power decompression, merging of incompatible test cubes
 13. Compaction of test responses
Objectives, placement of compactor, properties of ideal compactors, time compactors (signature analysis, arithmetic accumulation, counting), space compactors (XOR trees, error code-based), finite memory compactors, error models and aliasing, aliasing probability, Markov model, transient period
 14. Multiple input signature register (MISR)
Parallel data acquisition, multiple error injections, unknown (X) states and their sources, X states and signatures, X-masking schemes, X-bounding logic
 15. Compaction and diagnosis
Bypass mode, scan partitioning for diagnosis, identification of failing scan cells
 16. Built-in logic block observer (BILBO)
 17. BIST controller
Architecture, BIST session, logic BIST flow, parameters defined from BIST-ready process, user defined options, determined by synthesis tools, boundary scan and BIST
 18. Arithmetic and software BIST
 19. Memory BIST
Requirements, fault models, choice of algorithms, types of memories, configurations, operating speed, data retention, data backgrounds for word memories, parallel memory BIST, serial memory BIST, serial-parallel data interface trade-offs, memory BIST collar, shared controller and parallel test, parallel memory BIST collar, programmable algorithms, fault diagnosis for RAMs and ROMs
 20. Built-in self-repair.

9. Reliability and Design for Manufacturing

9.1. Abstract

CMOS technology scaling along with the resulting large variability of circuit performance has made post-silicon circuit and algorithmic level built-in test and adaptation/tuning almost a necessity for deeply scaled technologies. Currently, circuits are designed to tolerate worst-case process corners. In addition, circuits as well as the associated signal processing algorithms for real-time systems must be designed for worst case operating conditions (e.g. environmental noise). This forces designers to excessively guard band their circuits while using "aggressive" back-end algorithms to support the end application, resulting in unacceptable power-performance-yield tradeoffs. One way to tackle this problem is to design circuits and relevant signal processing algorithms that are "aware" of their environmental operating conditions and manufacturing process conditions and use this "self-awareness" to perform adaptation that conserve power while maximizing yield and reliability. Such self-adaptation involves incorporation of built-in test, diagnosis and tuning/adaptation mechanisms into the circuits and systems concerned. A key issue is that of test, diagnosis and tuning of complex circuit and system-level parameters that must be evaluated and traded off against one another during the adaptation process without access to complex external test instrumentation. This talk summarizes recent results obtained in the design of such highly reliable and manufacturable (in the face of process uncertainties) computing and communication systems and points to directions for future work in this area.

9.2. Schedule

Monday, May 24 : 8:00-12:30

9.3. Speaker

Abhijit CHATTERJEE

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9.3.1. Biography

Abhijit Chatterjee is a Professor in the School of Electrical and Computer Engineering at Georgia Tech.

He received his Ph.D in electrical and computer engineering from the University of Illinois at Urbana-Champaign in 1990.

Chatterjee received the NSF Research Initiation Award in 1993 and the NSF CAREER Award in 1995. He has received four Best Paper Awards and three Best Paper Award nominations.

In 1996, he received the Outstanding Faculty for Research Award from the Georgia Tech Packaging Research Center, and in 2000, he received the Outstanding Faculty for Technology Transfer Award, also given by the Packaging Research Center.

His research group received the Margarida Jacome award from the Berkeley Gigascale Research Center in 2007 for work on self-aware wireless systems. He has earlier served as a partner in NASA's New Millennium project.

Chatterjee has published over 300 papers in refereed journals and meetings and has 11 patents.

He is a co-founder of Ardext Technologies Inc., a mixed-signal test solutions company and served as Chairman and Chief Scientist from 2000 – 2002.

He is currently directing research at Georgia Tech in mixed-signal/RF design and test funded by NSF, SRC, MARCO-DARPA and industry and is a Fellow of the IEEE.

9.4. Syllabus

1. Definition of testing problem:
 - digital vs. analog testing
 - fault based vs. spec based
 - test flow for ICs
 - test flow for packages
 - what are we testing for?
2. Reliability models:
 - electromigration
 - hot carrier effects
 - reliability of deeply scaled devices, NBTI
 - temperature effects and wearout
 - digital vs. analog
 - system level reliability and mean time to failure

3. Design for manufacturability:
 - rule based design
 - optical proximity correction
 - tuning techniques
4. Introduction to Systems-on-Chip (SoCs):
 - test problems
 - test access techniques
 - IEEE P1500 standard
5. Contemporary spec based testing of analog and RF modules:
 - opamps
 - data converters
 - regulators
 - SerDes devices
 - RF modules and systems
 - common instruments used: rack and stack systems
 - common tests performed
 - spec test optimization methods
6. Fault modeling for analog and RF modules:
 - top down vs. bottom up modeling
 - catastrophic and parametric fault modeling
 - guardbanding and setting test limits
 - coverage models for analog
7. The alternate testing paradigm:
 - Core concepts
 - test generation
 - test methodology in production test
 - Application to precision opamps (industrial test case)
 - Application to CDMA LNA devices
 - Process diagnosis
8. System level alternate test and BIST:
 - Low cost testing of GSM transceiver
 - Low cost testing of OFDM transceiver
 - BIST using embedded sensors
 - BIST for nonlinearity, mismatch and EVM
9. Self-calibration techniques and adaptive systems:
 - one-shot tuning using alternate diagnostic tests
 - iterative test driven LMS based tuning
 - transmitter and receiver tuning against complex specs (EVM)
 - autonomous adaptation to process and environment
10. Self-test techniques for SoCs:
 - loopback testing of ADC and DAC modules
 - predicting individual parameters from loopback tests
 - spectral techniques applied to loopback test
 - on-chip sensors for low-cost test of RF modules
 - prototype hardware and chip measurement results
 - directions for self-adapting SoCs
11. Directions for future research:
 - error detection and fault tolerance
 - self aware systems.

10. Infrastructure IP for SOC

10.1. Abstract

In addition to the functional IP cores, today's SOC necessitates embedding a special family of IP blocks, called Infrastructure IP blocks. These are meant to ensure the manufacturability of the SOC and to achieve adequate levels of yield and reliability.

The Infrastructure IP leverages the manufacturing knowledge and feeds back the information into the design phase. This tutorial analyzes the key trends and challenges resulting in manufacturing susceptibility and field reliability that necessitate the use of such Infrastructure IP.

Then, it concentrates on several examples of such embedded IPs for detection, diagnosis and correction.

10.2. Schedule

Monday, May 24: 14:00-18:30 – Track A

10.3. Speaker

Yervant ZORIAN

Vice President & Chief Scientist

Virage Logic Corp.

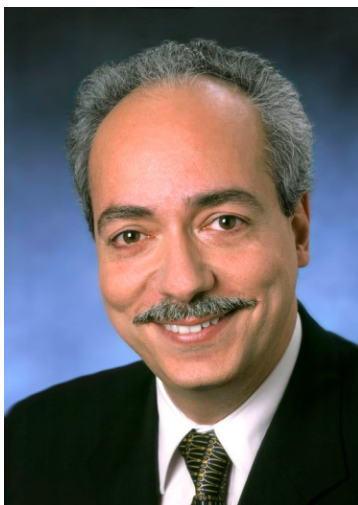
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10.4. Biography

Yervant Zorian is Chief Scientist and Vice President of Virage Logic Corp.

Previously, he was a Distinguished Member of Technical Staff at Bell Labs, Lucent Technologies, Test and Reliability Center of Excellence and the Chief Technology Advisor of LogicVision, Inc.

His activities include the areas of embedded core, SOC and System-in-Package DFT methodologies.

Zorian received an MSc degree from the University of Southern California, and a PhD from McGill University.

He served as the Vice President of IEEE Computer Society for Technical Activities, Conferences and Tutorials and the Editor-in-Chief Emeritus of IEEE Design & Test of Computers.

He founded and chairs the IEEE P1500 Embedded Core Test Standardization Working Group.

He has provided tutorials and courses at numerous conferences and academic programs (such as ITC, ICCAD, DATE, VTS, ETS, ATS, DAC, etc).

He has been granted over 20 patents in the domain of test and received a number of Best Paper Awards.

He is a recipient of IEEE Industry Pioneer Award.

10.5. Syllabus

- Introduction
- SoC Trends and Yield/Reliability Challenges
- Yield Optimization Loops
- Architecture of I-IP
- Embedded Process Monitoring IP
- Embedded Test & Repair IP
- Embedded Debug & Diagnosis IP
- Embedded Timing IP
- Embedded Fault Tolerance IP
- Conclusions.

11. Test of TSV-based 3D Stacked ICs

11.1. Abstract

The semiconductor industry is preparing itself for three-dimensional stacked integrated circuits (3D-SICs) based on Through-Silicon Vias (TSVs). TSVs are conducting nails which extend out of the back-side of a thinned-down die and enable the vertical interconnection to another die. TSVs are high-density, low-capacity interconnects compared to traditional wire-bonds, and hence allow for many more interconnections between dies, while operating at higher speeds and consuming less power. TSV-based 3D technologies enable the creation of a new generation of 'super chips' by opening up new architectural opportunities, allowing mixing of heterogeneous process technologies, at a smaller footprint and lower manufacturing cost. Due to their many compelling benefits, 3D-SIC technology is quickly gaining ground, and hence might help the semiconductor industry to extend the momentum of Moore's Law into the next decade.

Testing for manufacturing defects is considered by many as a major, still largely unresolved obstacle to make 3D integrated circuits a reality. There are concerns about testing cost, and even the feasibility of testing such TSV-based 3D-SICs.

However, the test community is waking up to address these challenges, testifying to the fact that 3D-SICs soon will hit the markets.

In this presentation, after a review of TSV-based technologies, we present a structured overview of the challenges in testing 3D-SICs, along with solutions as far as available today. Whereas these 'super chips' require most of today's advanced test and DfT approaches, they also have some unique challenges of their own. These include:

- development of new fault models and corresponding tests for thinned-die defects and TSV-based interconnects
- wafer probing on small and numerous micro-bumps and/or TSV tips under stringent damage requirements,
- handling of and probing on wafers with thinned-die stacks,
- further strengthening of the well-known modular test concept,
- the design, partitioning, and optimization of DfT architectures that span across multiple dies,
- optimization of the test flow for maximum effectiveness and lowest cost.

11.2. Schedule

Monday, May 24 : 14:00-18:30 – Track B

11.3. Speaker

Erik Jan MARINISSEN

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11.3.1. Biography

Erik Jan Marinissen received the MSc degree in Computing Science and the PDEng degree in Software Technology from Eindhoven University of Technology in 1990 and 1992, respectively.

He is currently a Principal Scientist at IMEC in Leuven, Belgium.

Prior to IMEC, he was with NXP Semiconductors and Philips Research, both in Eindhoven, The Netherlands.

Marinissen's research interests include all topics in the domain of test and debug of integrated circuits. He is a co-author of more than 125 journal and conference papers and a co-inventor of eight granted US and EU patent families.

He is a recipient of Best Paper Awards at the Chrysler-Delco-Ford Automotive Electronics Reliability Workshop in 1995, the IEEE International Board Test Workshop in 2002, and the Most Significant Paper Award at the IEEE International Test Conference in 2008. Marinissen served as an Editor-in-Chief of IEEE Std. 1500.

He serves on numerous conference committees, including Asian Test Symposium (ATS), Design, Automation and Test in Europe (DATE), European Test Symposium (ETS), International Test Conference (ITC), and VLSI Test Symposium (VTS), and on the editorial boards of IEEE 'Design & Test of Computers', IET 'Computers and Digital Techniques' (IET-CDT), and Springer's 'Journal of Electronic Testing: Theory and Applications' (JETTA).

He is a Senior Member of IEEE and a Golden Core Member of Computer Society.

11.4. Syllabus

1. Introduction
2. 3D Stacked ICs
 - Motivation
 - Application drivers
 - 3D manufacturing steps (incl. TSV formation, wafer thinning, and bonding)
 - Manufacturing options
3. 3D Test Flows
 - Wafer test and final test; pre-bond and post-bond testing; KGD and KGS testing
 - The value of pre-bond testing in W2W stacking
4. Modular Testing
 - Motivation for modular testing for 3D-SICs
 - Infrastructure for modular testing
5. 3D Test Contents

- Tests for new intra-die defects
- Tests for TSV-based interconnects
- 6. 3D Wafer Test Access
 - Challenges and solutions for pre-bond die testing
 - Challenges and solutions for post-bond stack testing
- 7. 3D DfT Architectures
 - Basic DfT architecture
 - The role of RPCT, TDC, and BIST
- 8. Conclusion
 - Tutorial summary
 - Evaluation with / by audience.

12. TSS@ETS 2010 Scientific Committee

Hans-Joachim WUNDERLICH (Chair) – Universität Stuttgart – Germany

Bernd BECKER – Universität Freiburg – Germany

Ondrej NOVAK – Technical University in Liberec – Czech Republic

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