Test Spring School @
EUROPEAN TEST SYMPOSIUM

Trondheim, Norway

May 20-23, 2011

Test Spring School at ETS'11

Rel. 007 - 3/11/2011

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1. School Presentation

The European Test Symposium offers a 3 day test spring school (TSS@ETS 2011) for Ph. D. and M. Sc. students which will introduce into modern test technology. Renowned experts will give lectures and will cover the main challenges of test and reliability of today's nanoelectronic systems.

Test and embedded test, manufacturability and robustness have to be considered by any system designer in order to come up with successful products. TSS@ETS offers the unique opportunity to learn about the leading edge of the state of the art in testing in a comprehensive and compact way. The school will give the opportunity to earn credits and a certificate by passing an exam online.

The school is organized in conjunction with ETS, and the last two lectures are open for the general ETS attendees without additional fee. TSS@ETS is offered to registered students at the low cost rate of appr. 400 EUR incl. food and the 3 day accommodation. The school is also available for professionals at higher rates, however priority is given to students on a first come – first serve basis as the number of attendees is strictly limited.

Hans-Joachim Wunderlich

Chair of the Steering Committee of ETS

Paolo Prinetto

Organization Chair

2. TSS@ETS Scientific Committee

- Bernd BECKER – Universität Freiburg – Germany
- Ondrej NOVAK – Technical University in Liberec – Czech Republic
- Paolo PRINETTO – Politecnico di Torino – Italy
- Michel RENOVELL – LIRMM – Montpellier – France
- Hans-Joachim WUNDERLICH (Chair) – Universität Stuttgart – Germany

3. Venue

Nidaros Pilgrim Centre (Nidaros Pilegrimsgård)
Kjøpmannsgata 1
N-7013 Trondheim
Norway

Tel: +47 73 52 50 00
Email: post@pilegrimsgarden.no
Web: http://www.pilegrimsgarden.no

4. Registration

Registrations should be done at:
http://www.iti.uni-stuttgart.de/tss2011

The registration fee for TSS@ETS'11 is NOK 2.200 (EUR 275) for PhD candidates and NOK 3.200 (EUR 400) for non PhDs. This covers the Test School with food and social events. Accommodation is not included in this fee.

Accommodation at The Nidaros Pilgrim Centre must be booked separately by sending an e-mail to pamelding@pilegrimsgarden.no. In the e-mail please introduce yourself as a TSS@ETS'11 participant and specify your arrival and leaving dates. Students that plan to share a room may send a common booking e-mail. You may also stay at The Pilgrim Centre during ETS'11 if you plan to attend the conference. The walking distance to the conference venue is shorter than from the city hotels. In this case you register to ETS without any hotel room.

Accommodation at The Pilgrim Centre (price per night, including breakfast):

Single (a twin bedded room with single occupancy)	650 NOK (ca. 81 EUR)
Twin bedded shared room	450 NOK (56 EUR)
Three bedded shared room	350 NOK (44 EUR)

5. Schedule

Friday, May 20	
16:00-18:00	Registration
19:00-	Welcome reception
Saturday, May 21	
7:30-8:00	Registration
8:00-8:15	Welcome Address (Hans-Joachim WUNDERLICH)
8:15-10:15	Each attendee introduces her/himself
10:15-10:30	Coffee break
10:30-12:45	Technology Trends in VLSI and Impact on Reliability and Test Shekhar BORKAR (part I)
12:45-14:00	Lunch
14:00-16:15	Technology Trends in VLSI and Impact on Reliability and Test Shekhar BORKAR (part II)
16:15-16:30	Coffee break
16:30-18:45	Wafer Level Reliability Screens and Adaptive Test Peter MAXWELL (part I)
19:00-	Social Dinner
Sunday, May 22	
8:00-10:15	Wafer Level Reliability Screens and Adaptive Test Peter MAXWELL (part II)
10:15-10:30	Coffee break
10:30-12:45	Understanding defects, diagnosis and variation Rob AITKEN (part I)
12:45-14:00	Lunch
14:00-16:15	Understanding defects, diagnosis and variation Rob AITKEN (part II)
16:15-16:30	Coffee break
16:30-18:45	Fault Models and Test Algorithms for Nanoscale Technologies Bernd BECKER (part I)
19:00-	Social Dinner
Monday, May 23	
8:00-10:15	Fault Models and Test Algorithms for Nanoscale Technologies Bernd BECKER (part II)
10:30-14:00	Checkout, Social event, Lunch, Transfer to ETS location
Track A 14:00-18:30	Embedded Memory Testing: Fault Models, Test Algorithms, MBIST and Industrial Results Said HAMDIOUI
Track B 14:00-18:30	Challenges in Design for Test and Fault Tolerance for Nanoscale Circuits Sybille HELLEBRAND

6. Course details

6.1. Technology Trends in VLSI and Impact on Reliability and Test

Saturday, May 21: 10:30-12:45 & 14:00-16:15
Nidaros Pilgrim Centre

– Speaker

Shekhar Borkar

Intel Corporation
2111 NE 25th Ave, JF2-04
Hillsboro, OR 97124
USA

Tel: +1 503 721 2871
E-mail: Shekhar.Y.Borkar@intel.com

Shekhar Borkar is an Intel Fellow, an IEEE Fellow, director of Academic Programs and Research, and director of Exascale research in Intel Labs. He holds MSEE from University of Notre Dame and MSc in Physics from University of Bombay. His research interests are low power, high performance digital circuits.

– Abstract

As technology continues to scale in the nanoscale regime, it's the same physics that helped you in the past, now poses major challenges in design, reliability, and test. Future designs will have to comprehend them, and incorporate reliability and test into the design from day one. Traditional system level reliability techniques will be ill suited and will have to morph towards resiliency. This course will address all of these challenges.

– Prerequisites

Fundamental knowledge of physics, electronics, and electrical engineering at the undergraduate level is required.

Suggested preliminary reading:

- Jan Rabaey: Low Power Design Essentials, Springer, ISBN 1558-9412
- Neil Weste and David Harris: CMOS VLSI Design, A Circuit and System Perspective, Third Edition and Addison Wesley, ISBN 0-321-14901-7
- James Segura and Charles F. Hawkins: CMOS Electronics, How it works, how it fails, IEEE Press, ISBN 0-471-47669-2

– Learning Outcomes

This course will familiarize you with the challenges of the nanoscale technologies, and effective design practices to overcome these challenges, both at the chip level as well as at the system level. You will be equipped with a good understanding of how to incorporate test and reliability into the design from day one, and to look forward to the paradigm shifts of resilient design for even more effective designs.

– Syllabus

1. Nanoscale Technologies: We will discuss the evolution of MOS transistors from yesterday's micro-scale to today's nanoscale regime, physics behind the scaling, and the same physics that now pose challenges for the future scaling. This includes subthreshold leakage, gate leakage, random and systematic variations, their causes, and the impact on VLSI chips.
2. VLSI Design Challenges of Nanoscale Technologies: We will discuss challenges associate with designing logic and circuits, considering major technological shifts discussed before. This includes design considerations for static, sequential, and storage circuit elements, with power management and delivery. We will further discuss the causes of faults, such as device aging, electromigration, as well as intermittent faults such as single event upsets, the errors caused by them, and design considerations to work around. We will especially focus on the reliability and test aspects from the design point of view.
3. System Design Challenges: Building systems with these components will be challenging too. System on a chip, as well as traditional board level system design will have to follow different design philosophy. We will discuss challenges associated at the system level, to provide sufficient IO bandwidth, power delivery and management, system reliability, and test - all within a reasonable power and cost envelope.
4. Designing for Reliability and Test: Having discussed the technological and design challenges we will focus on reliability and test aspects of the system. Traditional testing of components - as an afterthought - will be ineffective, and the future designs will have to incorporate testing as an integral part of the design effort. Traditional reliability solutions at the system level - such as N modular redundancy - too needs overhaul to morph into a new paradigm of system resiliency. We will discuss how designing for resiliency, with test and reliability in mind, will result in robust, reliable, and high yielding systems.

6.2. Wafer Level Reliability Screens and Adaptive Test

Saturday, May 21: 16:30-18:45
Sunday, May 22: 8:00-10:45
Nidaros Pilgrim Centre

– Speaker

Peter Maxwell

Aptina Imaging
3080 North First St
San Jose, CA 95134
USA

Tel: +1 408 660 2420
E-mail: pmaxwell@aptina.com

Peter Maxwell is an IEEE Fellow. He works for Aptina Imaging, where he is responsible for test and DFT for CMOS image sensors. He received the B.Sc. and M.Sc. (Honours) degrees from the University of Auckland, New Zealand, and the Ph.D. degree from the Australian National University.

His interests include test methodologies, design for testability, and their application for yield improvement and test time reduction. He has spent many years coordinating test experiments and was one of the first to widely publish industrial data on test effectiveness.

– Abstract

This tutorial discusses test methods and voltage stress approaches required to ensure cost effective defect screening to produce high quality, reliable products. With process variation having ever increasing significance, and design cannot completely compensate, test methods must deal with the variation. Adaptive test is being increasingly adopted to ensure high quality and reliability at a cost that cannot be achieved with traditional static testing.

The causes of process variation are discussed, highlighting increasing problems with more advanced technology nodes. A description of reliability measures is followed by a discussion of latent versus hard defects, and methods to accelerate latent defects so they can be detected at wafer/package test. Wearout and breakdown mechanisms are discussed in the light of stress techniques, which demonstrate limitations in stress effectiveness. Statistical based outlier screening methods are described, especially from the point of view of adaptive test.

A framework for adaptive test is presented and shows the many places where test data can be utilised. Some existing examples of adaptive test are described. These include its use for process ramp and debug, improved screening by modelling good die statistically and correlating fails of interest, and dynamic test elimination for analog circuits. Other benefits are discussed such as test cost reduction and operational test floor improvements.

Finally, several challenges are discussed. These include IT infrastructure, enabling of full traceability, developing tester-to/from-data analysis engine communication with significantly impacting test time, and the development of improved models and algorithms. The latter requires work in development of methods where the models are not fixed, better understanding of peripheral coverage and the associated quality impact of dropped or modified tests, and more encompassing fault coverage metrics, particularly for analog circuits.

– Prerequisites

Basic knowledge of electrical engineering, computer science and statistics.

Suggested preliminary reading:

- IEEE Design and Test special issue on latent defect screening, March-April, 2006 (several interesting papers).
- Production Data-Driven Statistical Testing, Session 13, Proceedings International Test Conference, 2005.
- P, Maxwell, "Adaptive Test Directions", Proceedings European Test Symposium, 2010, pp. 12-16.

– Learning Outcomes

Understand the topics given in detail below.

– Syllabus

1. Process complexity and variability. Implications of sub-wavelength printing techniques. A primer on optical proximity correction. Sources of variability. How lithography, gate oxide thickness and doping concentration translate into electrical parameter variations. Examples of effects of parameter variation and the limitations in design and modelling to deal with it.
2. Reliability units and measures. The traditional bathtub curve and how it is related to hazard rate and the Weibull distribution.
3. Hard versus latent defects and the need to accelerate latent defects to screen early life failures. Voltage and temperature acceleration and the reduced effectiveness with low supply voltage. How time dependent dielectric breakdown and hot carrier injection place constraints on voltage stress. Description and comparison of dynamic and enhanced voltage stress. Introduction to NBTI.

4. Components of wafer level reliability screen test suites. The concept of outlier screening. Parametric measurements and problems with fixed threshold techniques. Data driven testing and variance reduction. Methods to reduce variance by using predictors and residuals. Examples of outlier screens using statistical processing, part average testing, Iddq, MinVdd, Fmax. The benefits of adaptive limits.
5. Development of a framework for adaptive test showing how real-time analysis and optimization, and post-test analysis and disposition are integrated into various test steps. The use of feed-forward data from inline test and early test steps to later test steps and feed-back data from post-test statistical analysis to optimize testing of future products.
6. Examples of adaptive test. Its use for process ramp and debug, improved screening by modelling good die statistically and correlating fails of interest, and dynamic test elimination for analog circuits.
7. Stages of adaptive test. Static adaptation. Using real-time circuit response as input to algorithms which set test limits or test flows. Algorithm parameter determination and algorithm selection by characterization or by real-time response. New ideas in adaptation - adaptive on-chip sensors for NBTI aging.
8. Benefits of adaptive test. How the approach improves test cost, quality and reliability, yield learning, tester utilization and test floor efficiency.
9. Challenges. IT infrastructure, enabling of full traceability, developing tester-to/from-data analysis engine communication with significantly impacting test time, and the development of improved models and algorithms. development of methods where the models are not fixed, better understanding of peripheral coverage and the associated quality impact of dropped or modified tests, and more encompassing fault coverage metrics, particularly for analog circuits. Implications of multi-site test.

6.3. Understanding defects, diagnosis and variation

Sunday, May 22: 10:30-12:45 & 14:00-16:15
Nidaros Pilgrim Centre

– Speaker

Rob Aitken

ARM
Fellow, R&D
150 Rose Orchard Way
San Jose, CA, 95134
USA

Tel: +1 408 576 1315
E-mail: Rob.Aitken@arm.com

Robert C. Aitken is an R&D Fellow at ARM. His areas of responsibility include low power design, library architecture for advanced process nodes, and design for manufacturability. His research interests include design for variability, defect analysis, and fault diagnosis. He heads the San Jose branch of ARM's R&D operation which has taped out a number of chips, including 6 at or below the 32nm node. He has published over 70 technical papers, on topics ranging from the statistics of memory bit cell variability to the use of static current monitoring as a circuit testing and diagnostic mechanism (papers on the latter topic twice received the best paper award from the International Test Conference). Dr. Aitken joined ARM as part of its acquisition of Artisan Components in 2004. Prior to Artisan, he worked at Agilent and HP. He has given tutorials and short courses on several subjects at conferences and universities worldwide. He holds a Ph.D. degree from McGill University in Canada. Dr. Aitken is a senior member of the IEEE, and serves on a number of conference and workshop committees.

– Abstract

This tutorial gives a background on the nature of test in submicron processes, where a significant effort is devoted to measuring and understanding process variability, and care must be taken to choose where defect density leaves off and device variability begins. Three key technologies involved in this are diagnosis identifying failures and mapping them to physical causes, statistical design practices, which are used to tolerate expected amounts of variability, and test, which is used to eliminate variability that is outside of expected amounts.

– Prerequisites

Basic VLSI design, circuit design, test/ATPG

– Learning Outcomes

Attendees will learn the basics of sub-65nm process variability, DFM, fault diagnosis, and statistical design. Emphasis is placed on practical application over theoretical background, although the latter is provided where needed.

– Syllabus

1. Introduction and background

    - Class goal
    - What is DFX? Interaction of manufacturability, yield, variability, reliability and test
    - DFM background
    - Photolithography basics
    - Resolution enhancement technology
    - Physical variability
    - Defects and fault models
    - Manufacturability versus yield
    - Economics of yield
    - Classes of yield (systematic, defect-related, parametric, design-related)
    - Yield models and metrics

2. Diagnosis

    - Correlation, test, and measurement
    - Why do diagnosis
    - Scan chain diagnosis
    - Critical path tracing
    - Algorithmic IC diagnosis
    - Redundancy/Repair (memory and logic)

3. Variability

    - Design margin versus characterization
    - Statistical behavior (timing models, path-based, block-based)
    - Extreme value theory
    - SSTA, xOCV, and related concepts
    - Test for small delay defects

4. Putting it all together

    - Reliability issues (repair, aging, burn-in, materials)
    - Relationship of diagnosis, test, and variability
    - Areas for future research

6.4. Fault Models and Test Algorithms for Nanoscale Technologies

Sunday, May 22: 16:30-18:45
Monday, May 23: 8:00-10:45
Nidaros Pilgrim Centre

– Speaker

Bernd Becker

University of Freiburg
Faculty of Engineering
D-79110 Freiburg
Germany

Tel: +49 761 203 8140
E-mail: becker@informatik.uni-freiburg.de

Bernd Becker is an IEEE Fellow. He is a Full Professor at the Faculty of Engineering, University of Freiburg, Germany. Prior to joining University of Freiburg in 1995, he was with J.W.Goethe-University Frankfurt as an Associate Professor for "Complexity Theory and Efficient Algorithms".

The research activities of Bernd Becker have been primarily in the area of computer-aided design, test and verification of (digital) circuits and systems (VLSI CAD). A focus of his research is the development and analysis of efficient data structures and algorithms in VLSI CAD. The development of symbolic methods for test and verification of digital circuits and their integration in the industrial flow is one of the major achievements of his work. More recently, he has been working on verification methods for embedded systems and test techniques for nanoelectronic circuitry. He has published more than 200 papers in peer-reviewed conferences and journals and has been on the programme and organizing committees of numerous major international conferences.

Bernd Becker has been the holder of several research grants from DFG, BMBF and industry as well. Currently, he acts as the Co-Speaker of the DFG Transregional Collaborative Research Center "Automatic Analysis and Verification of Complex Systems (AVACS)" with project partners from University of Freiburg, University of Saarland, University of Oldenburg and Max Planck Institute of Computer Science.

– Abstract

Fault simulation and automatic test pattern generation (ATPG) are essential steps of test preparation for digital integrated circuits (ICs). While fault simulation is used to estimate the quality of an existing collection of test patterns (test set), ATPG is used to produce high-quality test patterns. Typical ATPG algorithms work iteratively: they generate pat-

terns, run fault simulation to determine whether the quality of the test set obtained so far is sufficient, and produce more patterns if required.

Both fault simulation and ATPG are defined with respect to a fault model. A fault is a model of a defect which could have occurred during the manufacturing of an IC. The modeling often implies abstraction, i.e., important behavioral details of low-level defective circuit behavior are not considered to reduce the complexity of fault simulation and ATPG. Different fault models are supposed to model different classes of actual defects with different degrees of accuracy.

In the age of Nanoscale Integration (NSI), state-of-the-art integrated circuits with gate length under 100 nm consist of hundreds of millions of transistors. This implies new challenges for their reliability. Typical defects encountered in today's technologies are so-called spot defects that may cause opens and/or shorts at one or more of the different conductive levels of the devices. Test generation for any type of defect is obviously not feasible due to the huge amount of CPU time and memory size required. Instead, test generation relies on fault models that are supposed to do both, i.e. to represent the defect behavior in an adequate way and to allow efficient ATPG and fault simulation for circuits of reasonable size.

The lecture starts by introducing basics of fault simulation and ATPG. Then we present modeling approaches and efficient test algorithms for fundamental NSI defect mechanisms like shorts and opens enabling the handling of industrial multi-million-gate circuits. We finish with a discussion of challenges for test algorithms in the area of variation aware testing.

– Prerequisites

Basic understanding of logic circuits and testing problems, introductory ideas of VLSI technology, see e.g. N. Jha, S. Gupta, "Testing of Digital Systems", Cambridge University Press, 2003, ISBN

– Learning Outcomes

In a first step fundamentals on testing problems with a focus on fault simulation and ATPG are recalled. Participants are aware of new challenges for the test of nanoscale electronics. In particular, they have a precise knowledge of more accurate models for shorts and opens used to better capture the actual physical defect mechanisms and the low-level behavior of the defective circuits. On the other hand side they understand how these models can be lifted to the logical level to allow efficient fault simulation and ATPG algorithms for industrially sized circuits. Finally, they have some first insight into the fundamental changes necessary for variation aware test algorithms.

– Syllabus

1. Basics
   Classical fault models, stuck-at faults, redundancy, fault simulation, automatic test pattern generation (ATPG), fault coverage, fault efficiency, defective parts per million (DPPM)
2. Defect-based test (DBT) and fault models
   Shorts, opens, aggressor-victim models, conditional stuck-at fault model, delay fault models, ATPG requirements, SAT-based ATPG
3. Test algorithms for resistive shorts
   Detection interval, fault coverage, , statistical definition, fault simulation and ATPG algorithms, extensions of the model to sequential circuits, feedback faults, non-nominal test conditions, and dynamic effects.
4. Test algorithms for opens
   Layout extraction and preprocessing, simulation of a given test set, untestability analysis, explicit test generation for opens, test set compaction, untestability analysis of aborted faults
5. Outlook: Test algorithms in variation-aware testing
   Variation aware fault simulation, multi-constraint ATPG, circuit analysis

6.5. Embedded Memory Testing: Fault Models, Test Algorithms, MBIST and Industrial Results

Monday, May 23: 14:00-18:45
TRACK A of ETS 2011

– Speaker

Said Hamdioui

Delft University of Technology
Computer Engineering Lab
Mekelweg 4, 2628CD
Delft
The Netherlands

Tel: +31 15 278 3643
E-mail: S.Hamdioui@tudelft.nl

Said Hamdioui received the MSEE and PhD degrees (both with honors) from the Delft University of Technology (TUDelft), Delft, The Netherlands. He is currently associate Professor at the Computer Engineering Lab. of TUDelft. Prior to joining TUDelft, Hamdioui worked for Microprocessor Products Group at Intel Corporation (in Santa Clara and Folsom, California), for IP and Yield Group at Philips Semiconductors R&D (Crolles, France) and for DSP design group at Philips/ NXP Semiconductors (Nijmegen, The Netherlands). He is the recipient of European Design Automation Association (EDAA) Outstanding Dissertation Award 2001, for his work on memory test techniques that have a wide-spread proliferation in the chip design industry; he is the winner of IEEE Nano and Nano Korea award at IEEE NANO 2010 - Joint Symposium with Nano Korea. He has received The Young Academy (DJA) of the Royal Netherlands Academy of Arts and Sciences (KNAW) nomination in 2009.

Hamdioui has published one book and over 80 papers in refereed journals and conferences. His research interests include dependable nano-computing and VLSI Test (defect/fault tolerance, reliability, security, nano-architectures, Design-for-Testability, Built-In-Self-Test, 3D stacked IC test, memory test, etc). He serves on numerous conference committees and is a member of IEEE.

– Abstract

Embedded memories have become the fastest growing segment of Systems on Chip (SoC) in recent years. According to the International Technology Roadmap for Semiconductors, embedded memories will continue to dominate the increasing SoC chip area in the future, approaching 94% within one decade. Hence, these memories will severely impact all aspects of SoC manufacturing including yield, quality and reliability. Additionally, nanotechnology is causing higher levels of device-parameter variations and new

failure mechanisms that are not yet well understood. Precise fault modeling to design efficient tests is therefore essential in order to keep the test cost and test time within economically acceptable limits, while keeping higher product quality.

The objective of this course is to provide PhD and MSc students with an overview of fault modeling and test design for memory devices. Traditional fault modeling and recent development in fault models for current and future technologies are covered. Systematic methods for designing and optimizing test patterns are presented, and supported by industrial results. Memory Built-In-Self Test, as a common industrial method to implement the test algorithms, is discussed. Last, future challenges in embedded memory testing (e.g., in fault modeling, test design) are highlighted.

– Prerequisites

It is recommended to read about the semiconductor memory architectures; especially SRAMs and DRAMs. The main blocks (e.g., address decoders, the memory cell array, etc) forming a memory system and how the operations (i.e., read and write) are performed should be known and understood. Any paper or book covering the functionality of semiconductor memories can provide this basic knowledge.

– Learning Outcomes

Upon the completion of the course, the attendee will:

- have a good knowledge of practices in memory testing,
- understand the major types of memory faults,
- know which tests should be performed to target each fault class,
- have a feeling of the effectiveness of each test,
- have the capability to develop new tests for any observed new faulty behavior and optimize them for specific application,
- understand how to design a Memory BIST,
- choose appropriate test strategy to achieve a high fault coverage with the minimum cost, and
- get insight into the direction and future of memory testing.

– Syllabus

1. Motivation

    - Quality versus reliability
    - Importance of (memory) testing

2. Memory Fault Models

    - Traditional fault models
    - Advanced fault models

3. Test Algorithms

    - Traditional tests
    - March tests
    - Fault-primitive based tests

4. Industrial Test Results
5. Memory Built-in-Self Test (MBIST)

    - MBIST requirements
    - Traditional MBIST architectures
    - Advanced MBIST architectures

6. Future challenges

6.6. Challenges in Design for Test and Fault Tolerance for Nanoscale Circuits

Monday, May 23: 14:00-18:45
TRACK B of ETS 2011

– Speaker

Sybille Hellebrand

University of Paderborn
Institute of Electrical Engineering and Information Technology, Computer Engineering Group
Warburger Str. 100
33098 Paderborn
Germany

Tel: +49 5251 60 3002
E-mail: sybille.hellebrand@uni-paderborn.de

Sybille Hellebrand received her Diploma degree in Mathematics from the University of Regensburg, Germany, in 1986. In the same year she joined the Institute of Computer Design and Fault Tolerance at the University of Karlsruhe, Germany, where she received the Ph. D. degree in 1991. Then she was as a postdoctoral fellow at the TIMA/IMAG-Computer Architecture Group, Grenoble, France. From 1992 to 1997 she continued as an assistant professor at the University of Siegen, Germany. Before completing her Habilitation and changing to the Division of Computer Architecture at the University of Stuttgart, Germany, in 1997, she spent several months as a guest researcher with Mentor Graphics Corporation in Portland, Oregon, USA. In 1999 she moved to the University of Innsbruck in Austria as a full professor for Computer Science. During her time in Innsbruck she was the head of the Institute of Computer Science from 2001 to 2004. Since December 2004, Sybille Hellebrand holds a chair in Computer Engineering at the University of Paderborn, Germany, and since 2006 she is also the head of the Institute of Electrical Engineering and Information Technology.

Her main research interests include test and diagnosis of micro-electronic systems, in particular built-in test, built-in diagnosis and built-in repair for systems-on-a-chip and networks-on-a-chip, as well as design and synthesis of testable and reliable circuits and systems. She has published numerous papers in international conferences, workshops, and journals. Besides her activities in several program committees, she serves as an associate editor for IEEE Design and Test and the Journal of Electronic Testing (JETTA).

– Abstract

Nanoscale integration comes along with an increased variability of circuit parameters as well as with growing soft error rates. To achieve acceptable yield and to ensure a reliable system operation in the field, a "robust" design must compensate both permanent and

transient faults to a certain extent. Testing becomes particularly difficult in this context, because different instances of a circuit may need different test sets and a robust design style makes it hard to distinguish between critical and non-critical failures during test. Moreover, a pass/fail-test is no longer sufficient, but the remaining robustness for system operation must be determined ("quality binning").

This tutorial shows how classical fault tolerant architectures can be used for yield and reliability improvement and also introduces emerging self-calibrating and adaptive architectures. Furthermore, the challenges of testing robust systems are discussed and specific DfT solutions are presented. Finally, techniques for analyzing the robustness properties of a circuit are explained.

– Prerequisites

- Basic knowledge about test and DfT, in particular built-in and embedded test
- Basic knowledge about fault tolerance

Suggested preliminary reading:

- Michael L. Bushnell, Vishwani D. Agrawal: Essentials of Electronic Testing for Digital, Memory, and Mixed-Signal VLSI Circuits; Kluwer Academic Publishers (Springer), 2000
- I. Koren and C. M. Krishna: Fault-Tolerant Systems; Morgan-Kaufman Publishers, San Francisco, CA, USA, 2007
- IEEE Design and Test: Special Issue on Design for Yield and Reliability, Vol. 21, No. 3, May/June 2004

– Learning Outcomes

- Understanding the challenges stemming from parameter variations and increased soft error rates
- Basic knowledge about design and DfT for robust architectures

– Syllabus

1. Introduction: New challenges for DfT and fault tolerance due to the increasing impact of parameter variations and soft errors.
2. Fault tolerance for yield and reliability improvement
3. New approaches for robust design (variation-tolerant, adaptive, self-calibrating, ...): basic ideas and architectures
4. Prerequisites for robust design:

    - Online monitoring, online error detection and correction
    - Monitoring of aging problems
    - Infrastructure for self-calibration

5. Test and DfT for robust design

    - Minimizing overtesting and yield loss
    - Test calibration
    - Design for "Quality Binning"

6. Robustness analysis