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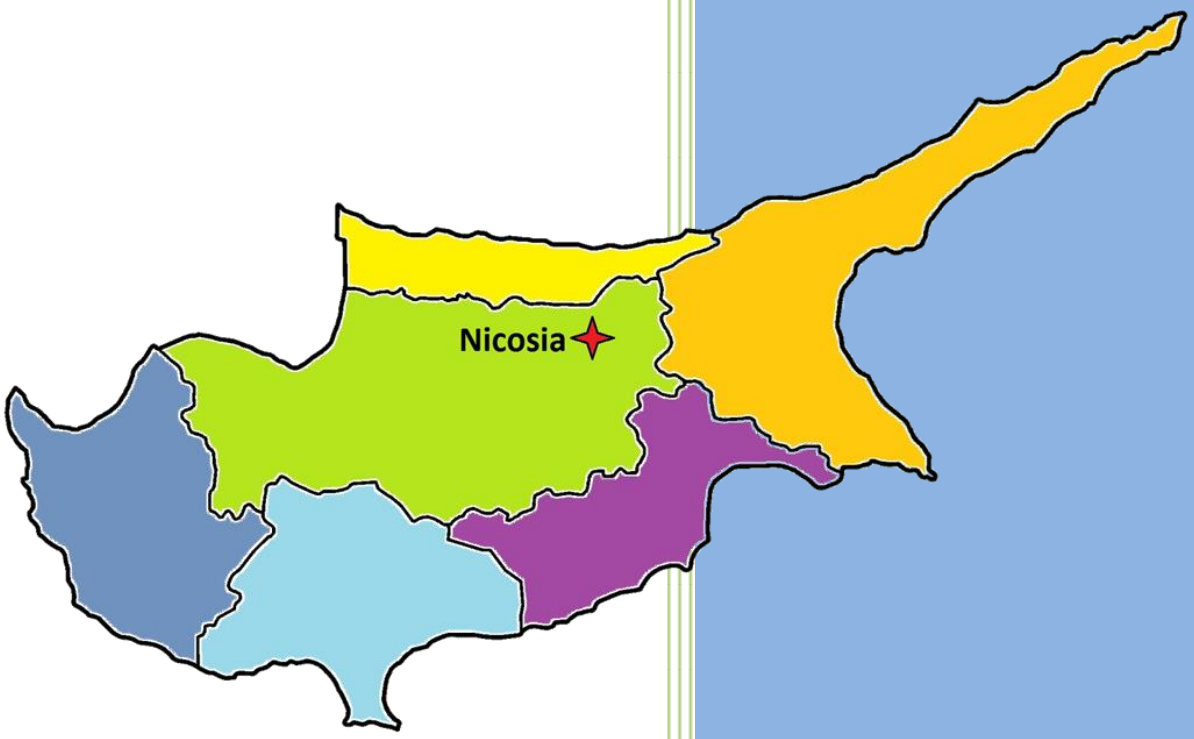
Test Spring School 17

2017

Test Spring School

Nicosia - Cyprus

May 19 - 22



Co-organized with the German DFG priority program SPP1500: "Dependable Embedded Systems“

Test Spring School 2017

Nicosia, Cyprus
May 19-22, 2017

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University of Cyprus

Scientific Committee:

TSS Chair:
Hans-Joachim WUNDERLICH (DE)

TSS Co-Chair:
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Matteo SONZA REORDA (IT)

Organizing Committee:

Ioana VATAJELU (FR)
Stelios NEOPHYTOU (CY)
Mike KOCHTE (DE)

Venue:

Classic Hotel Nicosia
94 Rigenis Str, 1513
Nicosia – Cyprus

Machine Learning for Test, Dependability and Fault Tolerance

The European Test Symposium offers a 3 day test spring school (TSS@ETS 2017, May 19 - 22) for Ph.D. and M.Sc. students who will be introduced into modern test, dependability and fault tolerance technology. Renowned experts will give lectures and will cover the main challenges of test and reliability of today's nanoelectronic systems. TSS@ETS offers the unique opportunity to learn about the leading edge of the state-of-the-art in modern test technologies in a comprehensive and compact way. The school will give the opportunity to earn credits and a certificate by passing an exam online. The school is open for registered students at an extremely low fee and welcomes also industrial professionals at a higher rate.

This year, emphasis is put on Machine Learning Techniques for Test, Dependability and Fault Tolerance. The school will show how most recent achievements in machine learning can be used to deal with the challenges of nanoscale integration. Wafer level screening, circuit and gate level approaches, alternate testing for RF, analog and mixed signal circuits, and system level test and diagnosis are the application areas for methods from data mining and artificial reasoning. Finally it is shown how these techniques implemented within a system will provide self-awareness and resilience against bugs and attacks.

The school is organized in conjunction with ETS 2017, and the last two lectures are open for the general ETS attendees without additional fee. It is also associated with the German DFG priority program SPP1500: "Dependable Embedded Systems".

TSS Chair
Hans-Joachim WUNDERLICH

TSS Co-Chair
Lorena ANGHEL

Registration:

The registration site opens on ***February 1st 2017***. The early registration deadline is ***April 10th, 2017***. After this date, accommodation cannot be guaranteed. Priority is given on a first-come first-served basis, as the number of attendees is strictly limited. Please register as soon as possible through the website at:
http://www.ets17.org.cy/tss/registration/

Package	Early Registration**	Late Registration
Student*	€ 370	€ 420
Industrial Professional	€ 700	€ 770

* University membership required
** The deadline for Early Registration is April 10th 2017

The package of TSS 2017 includes:

- 3 nights in shared double room (twin beds);
- Meals: 3 breakfasts, 3 lunches, 3 dinners (one with welcome reception) and coffee breaks;
- 2 social events including transport;
- Transport to ETS venue on 22 May 2017;
- Access to Test Spring School material & WiFi access.

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Machine Learning for Test, Dependability and Fault Tolerance

Lecture 1: Fundamental Machine Learning Techniques

Marios Polycarpou

Bio: Marios Polycarpou is a Professor of Electrical and Computer Engineering and the Director of the KIOS Research Center for Intelligent Systems and Networks at the University of Cyprus. He received undergraduate degrees in Computer Science and in Electrical Engineering, both from Rice University, USA in 1987, and the M.S. and Ph.D. degrees in Electrical Engineering from the University of Southern California, in 1989 and 1992 respectively. His teaching and research interests are in intelligent systems and networks, adaptive and cooperative control systems, computational intelligence, fault diagnosis and distributed agents. Dr. Polycarpou has published more than 280 articles in refereed journals, edited books and refereed conference proceedings, and co-authored 7 books. He is also the holder of 6 patents.

Prof. Polycarpou is a Fellow of IEEE and has served as the President of the IEEE Computational Intelligence Society (2012-13). He has served as the Editor-in-Chief of the IEEE Transactions on Neural Networks and Learning Systems between 2004-2010. He has participated in more than 60 research projects/grants, funded by several agencies and industry in Europe and the United States, including the prestigious European Research Council (ERC) Advanced Grant. Prof. Polycarpou is the recipient of the 2016 IEEE Neural Networks Pioneer Award.

Abstract:

During the last few years, machine learning has emerged as a key technology for allowing computers to derive useful insight from available data. This is achieved through specialized machine learning algorithms that process the data and provide useful information to the user or facilitate automated decisions for complex systems. Machine learning has been applied to a wide variety of applications, including medicine, self-driving cars, speech and image recognition, military, finance, etc. The importance of machine learning is likely to grow in the coming years as a way of handling the increasing volume, velocity and variety of available data. This session will provide an introduction to machine learning and present some of its fundamental algorithms. Specifically, the following machine learning concepts and methods will be introduced: linear regression; neural networks; support vector machines; unsupervised learning; fuzzy systems; and evolutionary computation.

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Lecture 2: Wafer Level Screening Techniques

John Carulli

Bio: John Carulli leads the Test organization at GLOBALFOUNDRIES Fab8 in Malta, NY working on leading edge CMOS technologies. He previously had 21 years at Texas Instruments where he was a Distinguished Member of the Technical Staff. While in the Analog Engineering Operations organization he led test and design data mining methods targeted at test cost reduction. Prior to that in the Silicon Technology Development organization, he was the Manager of the Product Reliability group responsible for product and design reliability activities for new technology development. John holds 7 US Patents. He has over 50 publications in the areas of reliability, test, and process development. He is co-recipient of two Best Paper Awards and two Best Paper Nominations working in close collaboration with university partners. John serves on the organizing or program committees of several conferences including the International Test Conference, VLSI Test Symposium, and European Test Symposium. He is a Senior Member of IEEE. He received his B.S.E.E. and M.S.E.E. degrees from the University of Vermont in Burlington, VT. His research interests include product reliability, outlier analysis, machine learning, performance modeling, logic diagnosis, and security.

Abstract:

For advanced CMOS technologies, we are now capable of creating billions to trillions of transistors per design. Following the economic path of Moore's law, we have built expertise to fool light as layout features needed to go sub-lithography. We have integrated new materials at an increasing pace to drive performance, power, and reliability. However, these advances brought and are continuing to bring significant challenges in dealing with variation. One of the key challenges in dealing with variation is understanding the impact on product reliability. This is becoming increasingly important to scale across differing business models and end applications. Automotive zero-defect requirements are moving more quickly to advanced CMOS technologies to meet the growing electronic content for safety, efficiency, and infotainment. Requirements for the internet-of-things (IOT) are also important business applications to dial in the right product reliability capability. The back-room compute and infrastructure needs have been around 100 defective-parts-per-million (DPPM) or below. It is not clear if the sensor fringe of IOT can attain aggressive DPPM at an economical cost point. In order to cover the above trends and observations, this class will unfold in two parts – Product Reliability & Wafer-Level Screening. To set the foundation, we will discuss the basics of reliability as applied to products. We will review the "bathtub curve" that outlines the reliability risk over time. An understanding of the main front-end and back-end reliability mechanisms will tie the material and layout control challenges in processing to the defect observability challenges in test. Once we understand the characteristics of a failure over time, we can see how wafer-level screening techniques can allow us to assess future failure risk. A critical component of these techniques is an understanding of how to leverage variation and statistics to our advantage. Published industry results will be used to show the benefits to augment traditional functional, structural, and spec-based testing approaches.

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Lecture 3: Circuit and Gate Level Learning Techniques

Mehdi Tahoori

Bio: Mehdi Tahoori is professor and Chair of Dependable Nano-Computing (CDNC) at the faculty of Informatics, Karlsruhe Institute of Technology (KIT) in Germany since 2009. Before that he was an associate professor of Electrical and Computer Engineering at Northeastern University, Boston, USA. From August to December 2015, he was a visiting professor at VLSI Design and Education Center (VDEC), University of Tokyo, Japan. He was also a research scientist at Fujitsu Laboratories of America in Sunnyvale California from 2002 to 2003. He received his Ph.D. and M.S. in Electrical Engineering from Stanford University in 2003 and 2002, respectively, and B.S. in Computer Engineering from Sharif University, Iran, in 2000.

He has published more than 250 conference and journal papers and holds several patents on various aspects of emerging technologies for computing and resilient system design. He is on the organizing and technical program committee of various design automation, test, and reliability conferences and workshops. He is an associate editor of ACM Journal of Emerging Technologies for Computing, associate editor for IEEE Design and Test Magazine, coordinating editor for Springer Journal of Electronic Testing (JETTA), and associate editor of IET Computers and Digital Techniques. He was the recipient of National Science Foundation CAREER Award. He received a number of best paper nominations and awards at various conferences.

Abstract:

With increasing the complexity of digital systems and the use of advanced nanoscale technology nodes, various process and runtime variabilities threaten the correct operation of these systems. The interdependence of these reliability detractors and their dependencies to circuit structure as well as running workloads makes it very hard to derive simple deterministic models to analyze and target them. As a result, machine learning techniques can be used at circuit and gate level to extract useful information which can be used to effectively monitor and improve the reliability of digital systems. These learning schemes are typically performed offline on large data sets in order to obtain various regression models which then are used during runtime operation to predict the health of the system and guide appropriate adaptation and countermeasure schemes. The purpose of this session is to discuss and evaluate various learning schemes in order to analyze the reliability of the system due to various runtime failure mechanisms which originate from process and runtime variabilities such as thermal and voltage fluctuations, device and interconnect aging mechanisms, as well as radiation-induced soft errors.

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Machine Learning for Test, Dependability and Fault Tolerance

Lecture 4: Applications of Machine Learning in the Design of Reliable and Trusted Analog/RF ICs

Yiorgos Makris

Bio: Yiorgos received the Diploma of Computer Engineering and Informatics from the University of Patras, Greece, in 1995 and the M.S. and Ph.D. degrees in Computer Engineering from the University of California, San Diego, in 1998 and 2001, respectively. After spending a decade on the faculty of Yale University, he joined UT Dallas where he is now a Professor of Electrical Engineering, leading the Trusted and RELiable Architectures (TRELA) Research Laboratory. His research focuses on applications of machine learning and statistical analysis in the development of trusted and reliable integrated circuits and systems, with particular emphasis in the analog/RF domain. He is also investigating error detection and correction methods for modern microprocessors, as well as novel computational modalities using emerging technologies. He is the 2016-2017 general chair and was the 2013-2014 program chair of the IEEE VLSI Test Symposium as well as the 2010-2012 program chair of the Test Technology Educational Program (TTEP). He is as an associate editor of the IEEE Transactions on Information Forensics and Security, the IEEE Design & Test periodical and the Springer Journal of Electronic Testing: Theory and Applications and he has also served as a guest editor for the IEEE Transactions on Computers and the IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, and as a topic coordinator and/or program committee member for several IEEE and ACM conferences. He is a Senior Member of the IEEE, a recipient of the 2006 Sheffield Distinguished Teaching Award and a recipient of the Best Paper Award from the 2013 Design Automation and Test in Europe (DATE'13) conference and the 2015 IEEE VLSI Test Symposium. His research activities have been supported by NSF, ARO, SRC, DARPA, Boeing, IBM, LSI, Intel, and Texas Instruments.

Abstract:

As electronics continue to penetrate every facet of contemporary life, the analog/RF integrated circuit (IC) market is experiencing unprecedented growth, with its current annual value standing at over $45B. With application domains mainly in wireless communications, real-time control, remote sensing, automotive and health, ensuring reliability and trustworthiness of analog/RF integrated circuits becomes paramount. This tutorial elucidates the role that machine learning and statistical analysis can play towards this end. Specifically, we will discuss (i) classification-based and regression-based test methods for asserting whether the performances of a fabricated analog/RF IC meet its specifications, (ii) statistical calibration methods for tuning the performances of each fabricated device through the use of on-chip knobs in order to increase yield, (iii) spatial and spatiotemporal analysis methods for achieving test time reduction by predicting the performances of a chip based on the performances of other chips in the same wafer or other wafers in the same lot, (iv) statistical side-channel fingerprinting methods for detecting malicious circuit inclusions (a.k.a. hardware Trojans) in wireless cryptographic ICs and for differentiating between genuine and counterfeit chips, (v) the design of on-chip analog neural networks for enabling post-deployment built-in self-test, self-repair and self-trust evaluation, and (vi) statistical methods for attesting the fabrication facility wherein a chip was manufactured. Results from industrial test data and measurements from custom-designed analog/RF ICs will be used to demonstrate effectiveness of machine learning in these applications.

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Lecture 5: Machine Learning Techniques for System Level Test and Diagnosis

Krishnendu Chakrabarty

Bio: Krishnendu Chakrabarty received the B. Tech. degree from the Indian Institute of Technology, Kharagpur, in 1990, and the M.S.E. and Ph.D. degrees from the University of Michigan, Ann Arbor, in 1992 and 1995, respectively. He is now the William H. Younger Distinguished Professor of Engineering in the Department of Electrical and Computer Engineering at Duke University. Prof. Chakrabarty is a recipient of the National Science Foundation CAREER award, the Office of Naval Research Young Investigator award, the Humboldt Research Award from the Alexander von Humboldt Foundation, Germany, the IEEE Transactions on CAD Donald O. Pederson Best Paper award (2015), and 11 best paper awards at major IEEE conferences. He is also a recipient of the IEEE Computer Society Technical Achievement Award (2015) and the Distinguished Alumnus Award from the Indian Institute of Technology, Kharagpur (2014). He is a Research Ambassador of the University of Bremen (Germany) and a Hans Fischer Senior Fellow at the Institute for Advanced Studies, Technical University of Munich, Germany. Prof. Chakrabarty's current research interests include: testing of integrated circuits and systems; microfluidic biochips and cyberphysical systems; enterprise systems and smart manufacturing. He is a Fellow of ACM, a Fellow of IEEE, and a Golden Core Member of the IEEE Computer Society. He holds eight US patents, with several patents pending. Prof. Chakrabarty served as the Editor-in-Chief of IEEE Design & Test of Computers during 2010-2012 and ACM Journal on Emerging Technologies in Computing Systems during 2010-2015. Currently he serves as the Editor-in-Chief of IEEE Transactions on VLSI Systems. He is also an Associate Editor of IEEE Transactions on Computers, IEEE Transactions on Biomedical Circuits and Systems, IEEE Transactions on Multiscale Computing Systems, and ACM Transactions on Design Automation of Electronic Systems.

Abstract:

The gap between working silicon and a working board/system is becoming more significant and problematic as technology scales and complexity grows. The result of this increasing gap is failures at board and system level that cannot be duplicated at the component level. These failures are most often referred to as "No Trouble Found" (NTF). The result of these NTFs can range from higher manufacturing cost, and failure to get the product out of the door. The problem will only get worse as technology scales and will be compounded as new packaging techniques such 2.5D/3D extend and expand Moore's law. The speaker will describe the nature of this problem and present recent advances in using machine-learning techniques to facilitate accurate and rapid board repair. In particular, the speaker will describe how techniques such as artificial neural networks, support-vector machines, decision trees, and information-theoretic analysis can be used for addressing root cause identification in boards and systems. He will present Imputation methods that allow us to carry out reasoning using incomplete data. Methods for knowledge discovery and knowledge transfer for early-stage diagnosis will also be presented. The presentation will include a number of case studies using telecom boards from high-volume manufacturing.

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Lecture 6: Self-Awareness and resilience against faults, bugs and attacks

Axel Jantsch

Bio: Axel Jantsch received the Dipl.Ing. and Dr. Tech. degrees from TU Wien, Vienna, Austria, in 1988 and 1992, respectively. He was with Siemens Austria, Vienna, Austria, as a system validation engineer from 1995 to 1997. From 1997to 2002 he was an associate professor and from 2002 to 2014 he was full professor of Electronic Systems Design at the Royal Institute of Technology (KTH), Stockholm, Sweden. Since 2014 he has been professor of Systems on Chip at TU Wien. He has published about 300 papers in international conferences and journals and one book in the areas of Systems on chip, networks on chip and embedded systems. He has served on a large number of technical program committees of international conferences, such as FDL, DATE, CODES ISSS, SOC, NOCS, and others. He has been the TPC Chair of SSDL/ FDL 2000, the TPC Co-Chair of CODES ISSS 2004, the General Chair of CODES ISSS 2005, and the TPC Co-Chair of NOCS 2009. From 2002 to 2007, he was a subject area editor for the Journal of System Architecture. He is on the editorial board for IEEE Design and Test and for the Leibniz Transactions on Embedded Systems. He is a member of the IEEE. His main research interest is on networks on chip and self-awareness in systems on chip and embedded systems.

Abstract:

The traditional paradigm of design and validation of electronic systems is to fully and precisely specify a system, and then design, implement and verify it according to this specification. This paradigm has achieved operational systems with billions of transistors, wonderfully sophisticated functionality and with amazing precision. However, with the further increase in complexity, higher demands on adaptability, resilience and autonomy, and the deployment in less predictable and changing environments, alternative paradigms of design and operation are explored. Self-awareness describes the capability of a system to monitor its own state, its performance and its integrity. Equipped with an accurate assessment of its own situation it can identify aberrations for expectations which may be due to faulty hardware, ill designed software or malicious attacks.

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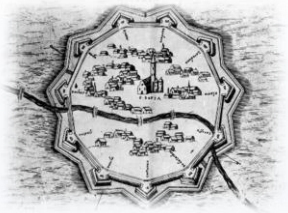

Venue: Nicosia, Cyprus

Nicosia, (Lefkosia), is the largest city on the island of Cyprus and the capital and seat of government of the Republic of Cyprus, and as such is the farthest southeast of all EU member states' capitals. Apart from its legislative and administrative functions, Nicosia has established itself as the island's financial capital and its main international business centre.

Having being continuously inhabited for over 4,500 years, Nicosia is one of the oldest cities in Eastern Mediterranean and Middle East. Today, the city is a sophisticated and cosmopolitan place in the area, rich in history and culture and combines its historic past with the amenities of a modern city. Nicosia was a city-state known as Ledra or Ledrae in ancient times. Ledra in Hellenic and Roman times was a small, unimportant town, also known as Lefkothea. The Greek name of Nicosia, "Lefkosia", probably comes from Lefkos, son of Ptolemy I of Egypt, who rebuilt the city in the 3rd century B.C.

Still known as Lefkosia, the city became the island's capital around the 10th century. It had grown in importance because of threats to the coastal cities Paphos and Salamis, which made many people flee to the centrally located Lefkosia. In 1567, the Venetians took over the island, and built the fortification with the eleven bastions, that one can still see today. Nicosia though, has a history dating long before that period, and has been the capital of the island since 1192, when a French Royal family, the Lusignans, made it their capital. They built an important number of monuments, such as churches, monasteries, palaces, etc. Nicosia had 250 churches and the town was much larger than the one built by the Venetians, who had destroyed a large number of original buildings to construct the fortifications.

Currently, the city within the walls retains a very strong folkloric character that combines, commercial and cultural activities to give a real sense of the old city, its architectural character and its tradition.

TSS Venue:

Classic Hotel Nicosia
94 Rigenis Str, 1513, Nicosia – Cyprus;
Phone: + 357 22664006; E-mail: info@classic.com.cy
Website : http://www.classic.com.cy/

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Social Events

Walled City Guided Tour:

Saturday 20 May 2017,
18:00 – 22:30.
Pass through most important monuments of the city.
Dinner with traditional local cuisine.

Beach Party at Larnaca

Sunday 21 May 2017,
17:00 – 22:30
Organized activities by the beach.
Dinner on the beach.

Contact:

For any further information please contact:

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